**EE307 Digital Electronics and Integrated Circuits**

**Class Final**, **Winter 2016**

**NAME:**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

No calculators. Only use documents on the PolyLearn page that I prepared for this exam.

No cheating or I reserve the right to fail you in this class and report you.

Show work where asked (or no credit!).

Rules:

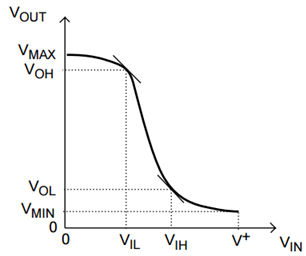
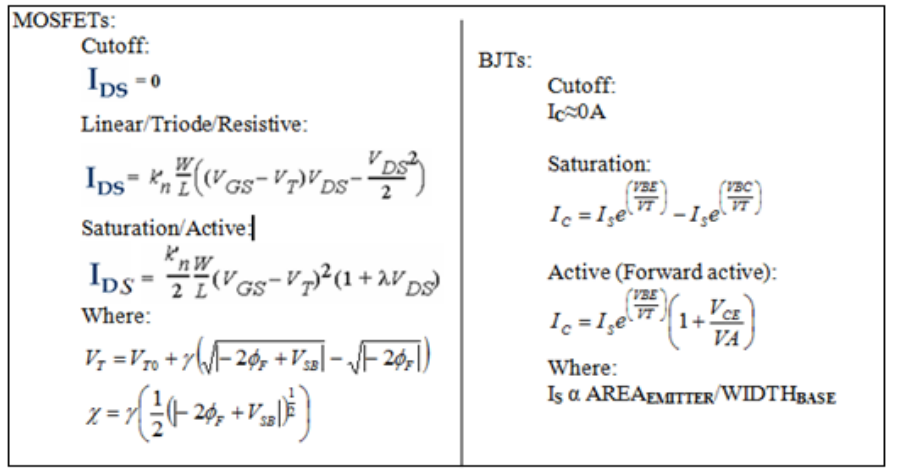
**I will not talk about this exam with anyone that hasn’t taken it yet.**

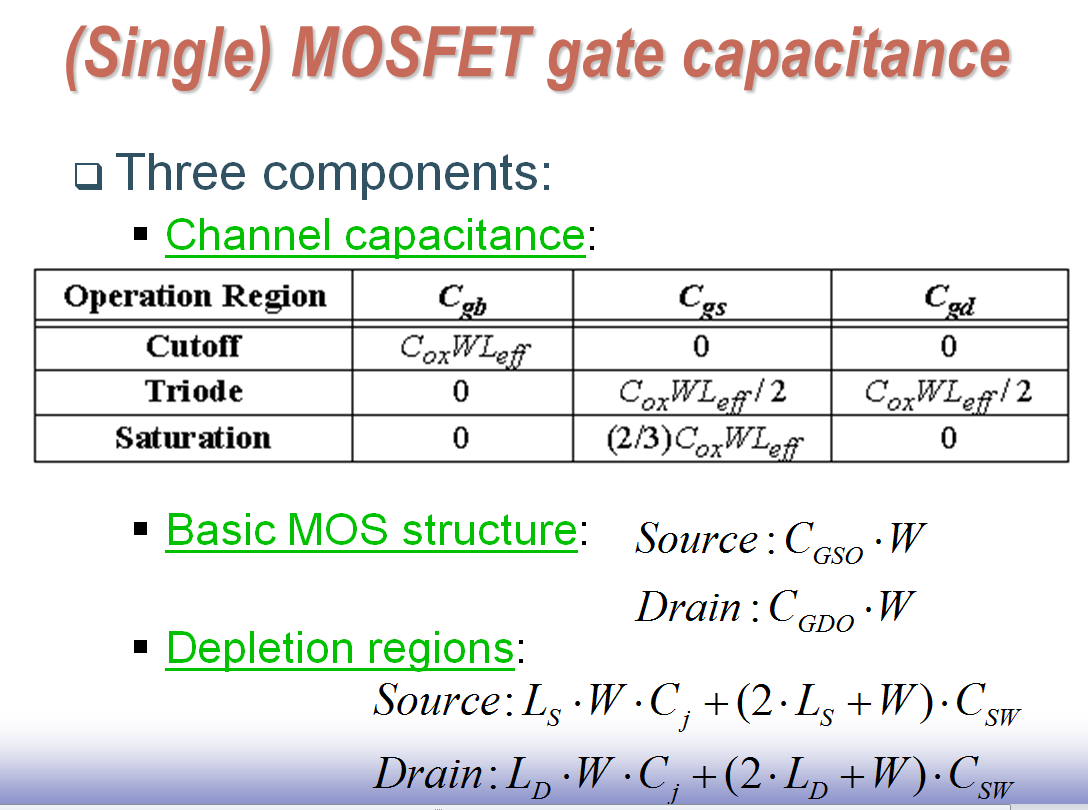
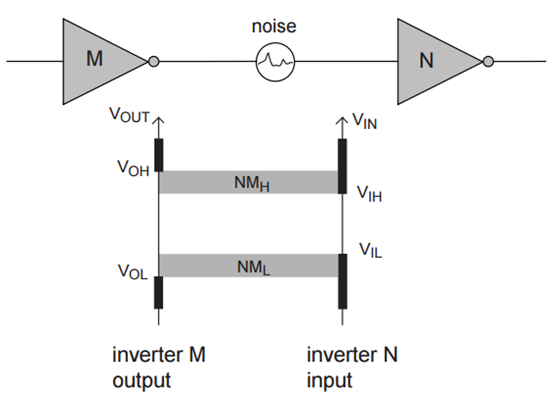
**Signature:**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

|  |  |  |
| --- | --- | --- |
| Question | Pts | Score |
| 1a-b | 6 |  |
| 2 | 5 |  |
| 3a-h | 48 |  |
| 4 | 30 |  |
| 5a-b | 12 |  |
| 6a-j | 34 |  |
| 7a-e | 20 |  |
| Total | 155 |  |
|  |  |  |
|  |  |  |
|  |  |  |

Delay: 

Power: 

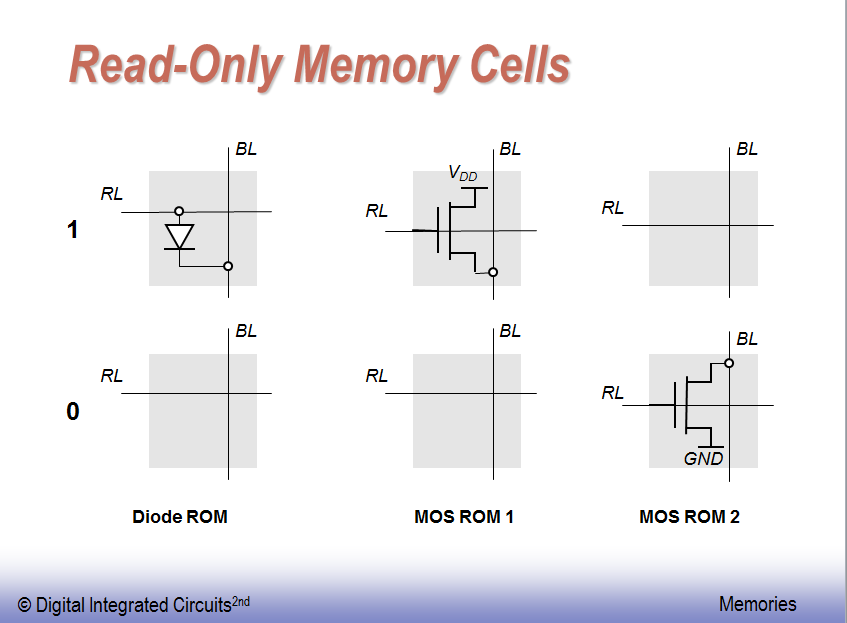
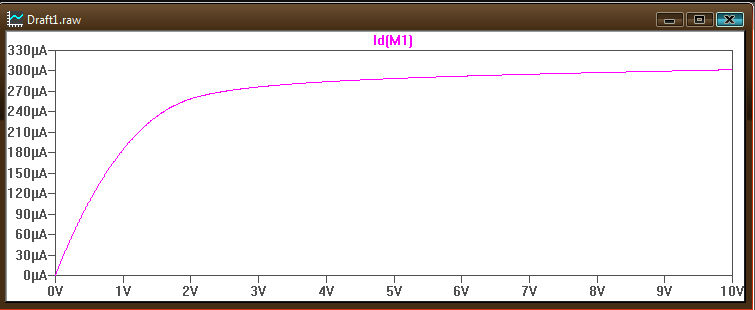


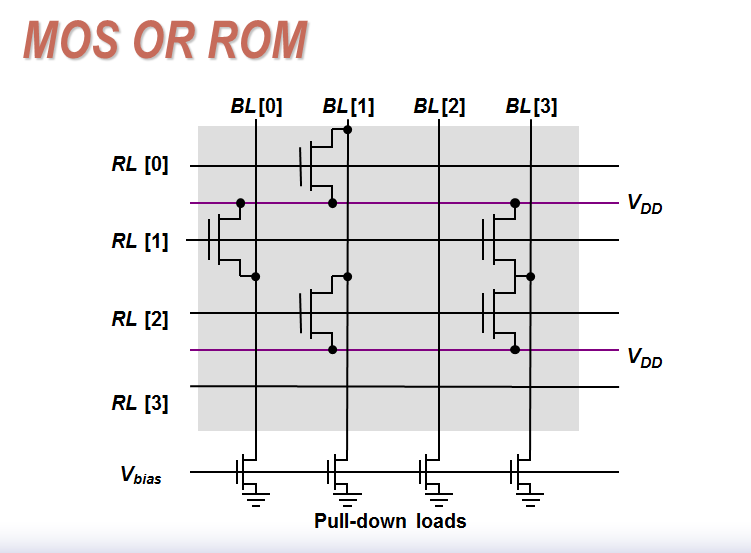
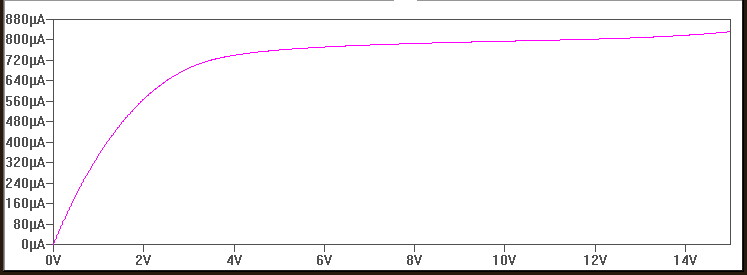
Definition: VTC or transfer characteristics: Vout on Y-axis, Vin on X-axis. More generally: Input on X-axis, output on Y-axis.

Definition of “Forward active” for BJTs includes both VCEsat and PN junction requirements.

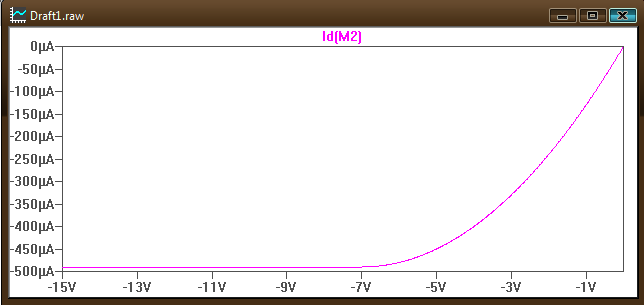
Memory: NMOS: VTC1 (Extrapolate to 15V)

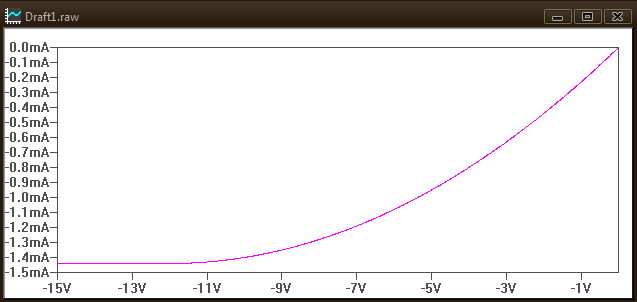
npn: VTC2

PMOS: VTC3



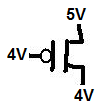
pnp: VTC4



Exam:

1. Regions of operation. Questions 1a through question 1b assume: VT=0.55V, VBE**ON**=0.65V, VBC**ON**=0.45V, and VCESAT=0.2V. (Total: 6 pts – 3pts each)
   1. Draw a PMOS. Draw in voltages at the terminals that would put the PMOS in the active region.

**ANSWER:**

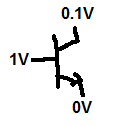


VS-VG>0.55V

(VS-VG)-VT < VDS

* 1. Draw an npn. Draw in voltages at the terminals that would put the npn in the linear region.

**ANSWER:**



VB-VE > 0.65V

VC-VE < 0.2V

1. Power: What is the frequency where an MCML’s power would become less than the power used by a MOSFET inverter? I am looking for an equation. Not a number. Frequency=….

**ANSWER:**



You want to find the frequency when the power of MCML is less than a CMOS inverter:



Solve for frequency:



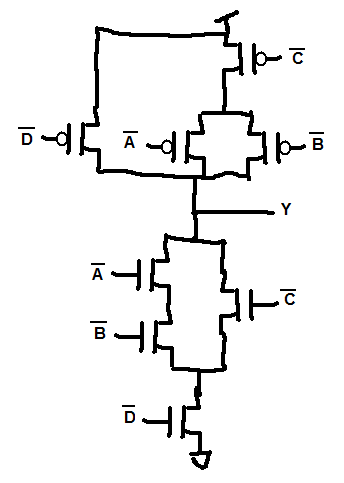
1. Logic families part 1: All questions in this section refer to the following equation: . Assume you have inverted signals available: So you have both “A” and “” available.
   1. Show work to convert this equation to an equation useful for designing the pulldown network of a CMOS logic circuit. Make sure to use parenthesis when there can be any confusion.

**ANSWER:**



* 1. Draw the complete schematic of the CMOS circuit. Draw a circle around any blocks you may use in future questions and label them.

**ANSWER:**

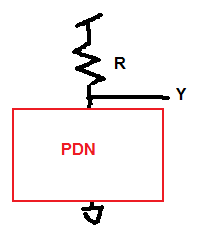


PUN

PDN

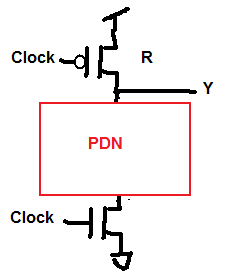
* 1. Draw an RTL circuit. You can use a black box for the parts that you are reusing from part 3b. Make sure to label them so I know which block you are reusing. Draw in the circuit components (resistors and/or transistors) that are new.

**ANSWER:**



* 1. Draw a dynamic logic circuit. You can use a black box for the parts that you are reusing from part 3b. Make sure to label them so I know which block you are reusing. Draw in the circuit components (resistors and/or transistors) that are new.

**ANSWER:**



* 1. Draw a domino logic circuit. Assume that two of the circuits you designed in part 3d are cascaded. You can use a black box for the parts that you are reusing from part 3b. Make sure to label them so I know which block you are reusing. Draw in the circuit components (resistors and/or transistors) that are new. Show all work to in finding any additional logic you may need.

**ANSWER:**

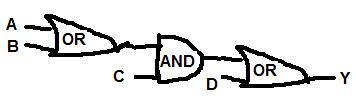


I misled the class a bit here. Since all the inputs are inverted, nothing needs to be done to the second block. Because this turned out to be a trick question I will be very generous.

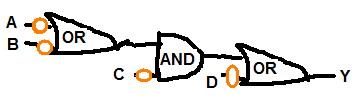
**IGNORE:** The second circuit’s logic needs to be calculated: 

I’ll use bubble pushing:

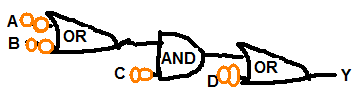
Original circuit:



Add inverters to the inputs:



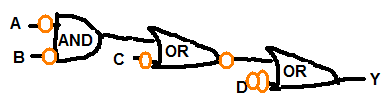
That changed the logic so add another bubble:



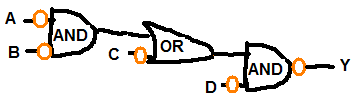
Now the logic is the same as the original but now has the same problem as the original circuit (precharge of the first circuit turns on the pulldown network of the second circuit) so bubble push one bubble through:



Then push through the center gate:



Then through the last gate:



Turning this into logic you get:



That gives you the pulldown logic for the second domino circuit which is the same as you started with….

* 1. Draw the OBDD (not simplified) and the ROBDD with leaves equal to ‘1’s and ‘0’s.

**ANSWER:** OBDD

0

1

0

1

0

1

11

1

0

1

1

1

0

1

1

1

ROBDD work:

0

1

0

1

0

1

11

0

1

1

1

0

1

1

0

1

0

1

11

0

1

1

0

1

1

0

1

0

1

11

0

1

1

**0**

**0**

**0**

**0**

0

1

**1**

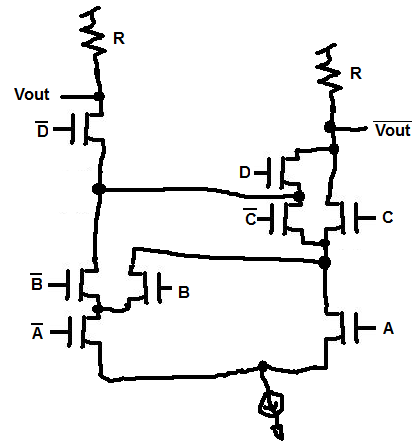
**1**

**1**

**1**

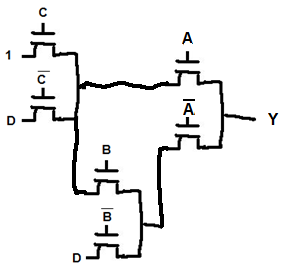
* 1. Draw the MCML from the ROBDD.

**ANSWER:**



* 1. Draw the pass transistor logic from the ROBDD. See if the leaves can be simplified over what you found in part 3c to help make the pass transistor logic circuit simpler.

**ANSWER:** Simplifying



**0**

**0**

**0**

D

1

**1**

**1**

**1**

**0**

**0**

**0**

**0**

0

1

**1**

**1**

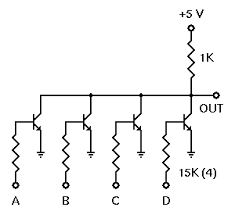
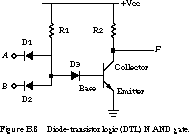
**1**

**1**

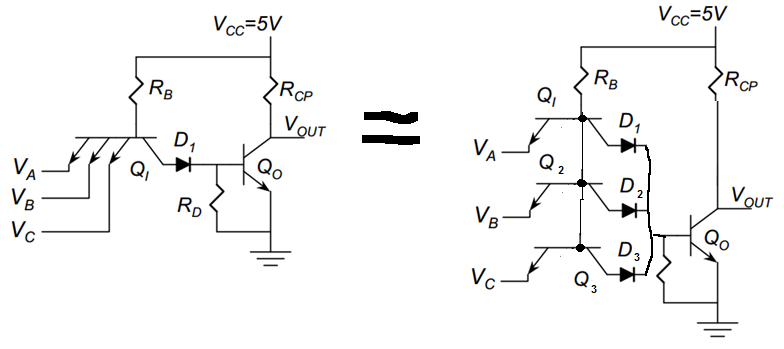
1. Logic families part 2: Fill in the following table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Circuit | Family name | Style name (Example: Ratioed logic) | Logic equation | When the output is low, is there high or low static power dissipation? |
| a) | DTL | Ratioed | NAND | High |
| b) | RTL | Ratioed | NOR | High |
| c) | TTL | Ratioed | NOR | High |
| d) | CMOS | Static | NOR | Low |
| e) | DL | Ratioed | (A+B) ∙ (C+D) | High |

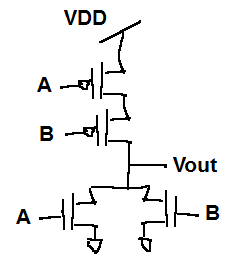
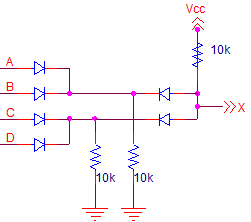
1. b)



c)



d) e)

1. Timing:

D0 Q0

Clock

D1 Q1

Delay

1ns < Delay < 3ns

|  |  |  |
| --- | --- | --- |
|  | Flip flop 0 | Flip Flop 1 |
| Hold time | 6ns | 5ns |
| Setup time | 7ns | 6ns |
| TclkQ | 3ns ≤ TclkQ ≤ 6ns | 8ns ≤ TclkQ ≤ 10ns |

* 1. What is the fastest this system can be run? (What is the minimum period that will make sure that there is never a failure due to setup time violations).

**ANSWER:**



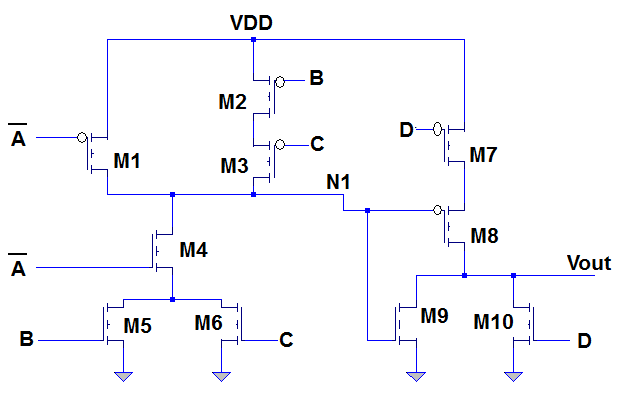
* 1. Can there be a hold time violation on this circuit? Show the math and say which path has the violation if there is one.

**ANSWER:**



There can be a hold time violation going from Q0 to D1.

1. Delays:



Circuit for question 6

* 1. What is the value at N1 when: A=B=C=D=0? (2pts)

**ANSWER:** N1 🡪 VDD

* 1. What is the value at Vout for the same inputs: A=B=C=D=0? (2pts)

**ANSWER:** Vout 🡪 GND

* 1. What is the value at N1 when: A=C=D=0 and B=1? (2pts)

**ANSWER:** N1 🡪 GND

* 1. What is the value at Vout for the same inputs: A=C=D=0 and B=1? (2pts)

**ANSWER:** Vout 🡪 VDD

* 1. What is the perceived capacitance (capacitance with Miller effect included) at N1? Use subscripts to show which transistor each capacitance belongs to. Transition described in question 6h. (6pts)

**ANSWER:** If they didn’t do the the right transition:

****

If they did the right transition:

****

* 1. Use the two point approximation on VTC3 (after cheat sheet stuff) to find Ron for a PMOS. No need to simplify. Just set up the equation. Assume VDD=15V. (4pts)

**ANSWER:** 

* 1. Use the one point approximation on VTC1 to find Ron for a NMOS. No need to simplify. Just set up the equation. Assume VDD=15V. (4pts)

**ANSWER:** 

* 1. What is the time constant for the transition caused by changing the inputs from A=C=D=0 and B=1 to A=B=C=D=0? (6pts) at N1.

**ANSWER:** 

* 1. Find either the equation for tr (rise time) or tf (fall time) - whichever is appropriate – for N1 for this change in inputs. (3pts)

**ANSWER:** 

* 1. Find either the equation for tpHL or tpLH - whichever is appropriate – for N1 for this change in inputs. (3pts)

**ANSWER:** 

1. Short answers:
   1. If the delay through an inverter is tp and there are 9 inverters in a ring oscillator, what is the period of the ring oscillator?

**ANSWER:**

9x2xtp = 18tp

* 1. What are the two main uses of a 555 timer?

**ANSWER:**

Clock, monostable

* 1. How does an output stage protect a logic circuit?

**ANSWER:**

It protects the voltage at the node while still being able to supply current to whatever the circuit is driving.

* 1. When would you use DRAM over SRAM?

**ANSWER:**

When you need a small area but aren’t too worried about speed.